The Handiman's Guide to MOSFET "Switched Mode" Amplifiers

Part 1

Introduction to Class C,D,E and F

by Paul Harden, NA5N

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Part 1 is a tutorial for using switching MOSFET's for QRP power amplifiers. Beginning with the standard Class C power amplifier, special emphasis is given to the Class D, E and F high efficiency modes.

Meet the MOSFET

MOSFET's have been used for years in QRP transmitters, but with an apparent level of mysticism as to how they really work. There are two main types of mosfet's: the linear RF mosfets, such as Motorola's "RF Line," and the more common switching mosfets. The **RF mosfets** are excellent, reliable devices for up to 30MHz, and some VHF versions. However, they cost $25–35 each or more, and beyond the budgets of most amateurs. **Switching mosfets** are far more common, such as the IRF510, available at hobby vendors and Radio Shack for about $1. These cheap switching mosfet's are the ones used in most home brew QRP transmitters, and the ones upon which this article focuses.

As the name implies, this family of mosfet's are designed to be *switches* -- that is, to primarily turn current on or off, just like a switch or relay. They are not perfect. Between the OFF and ON states, there is a linear region. Compared to standard bipolar transistors, mosfets have a narrower linear region. IRF510s, used for QRP Class C PA's, attempt to bias for this more restrictive linear region. However, if the device is accidentally driven into saturation, it causes excessive drain current and heating of the mosfet – and often failure. If you haven't blown up an IRF510 yet – you just haven't worked very hard at it!

The IRF series of switching mosfets were developed by International Rectifier. They make the "dies" for these mosfet's, marketing them under their own name (logo "I-R"), or selling the dies to other manufacturer's, such as Motorola and Harris, who merely adds the TO-220 packaging. Thus, no matter where you get your IRF510, you are getting the same device and can be assured of consistent operation.

The exception to this are some IRF510s sold by Radio Shack. Some are manufactured in Haiti that may or may not meet specs for maximum drain current, or at what gate voltage the device turns on and reaches saturation. To avoid legal problems with I-R, Radio Shack packages these mosfet "clones" under the part number IFR510 (not IRF510). An unrecognizable logo indicates a device manufactured off-shore.

Most power mosfets are made by stacking several dies in parallel to handle higher currents. The disadvantage is the capacitances add in parallel, which is why power mosfets have large input and output capacitances over single die devices. Mosfets made by vertically stacking the dies are called VMOS, TMOS, HexFets and other such names.

According to the I-R applications engineer, the IRF510 is their most widely sold mosfet. This is because it was developed by I-R in the 1970's for the automotive industry as turn-signal blinkers and headlight dimmers to replace the expensive electro-mechanical switches and relays. The good news is, this implies they will not be going away any time soon. In talking to International Rectifier, they were floored to find out QRPers were using them at 7MHz or higher. I faxed them some QRP circuits to prove it. Quite a difference compared to the 1Hz blink of a turn signal, or the 50kHz rate of a switching power supply!

BJT's vs. MOSFET's

Bipolar junction transistors (BJT) are forward biased with a base voltage about 0.7v (0.6v on most power transistors). Below 0.7v, the transistor is in *cut-off*: no collector current is flowing. Above 0.7v, collector current begins to flow. As you increase the base voltage (which is actually increasing base current), it produces an increase in collector current. This is the *linear region* – converting a small change on the base to a much larger change on the collector. This defines amplification. As you continue to increase the base voltage further, a point will be reached where no further increase in collector current will occur. This is the point of *saturation*, and the point of maximum collector current. The base voltage required to saturate the transistor varies from device to device, but typically falls in the 8v range for most power transistors used for QRP PA's. This is, actually, a fairly large dynamic range. A graph showing these regions is called the "transfer characteristics" of a device, as illustrated in **Fig. 1A**, showing a sample Class C input and output signal. Self-biasing is assumed, that is, the input signal is capacitively coupled to the base with no external (0v) bias.

MOSFETs work in a very similar manner, except the gate voltages that defines cut-off, the linear region, and saturation are different than BJT's. While it takes about 0.7v to turn on a BJT, it takes about 4v to turn on an IRF510 mosfet. The voltage required to cause drain current to start flowing is

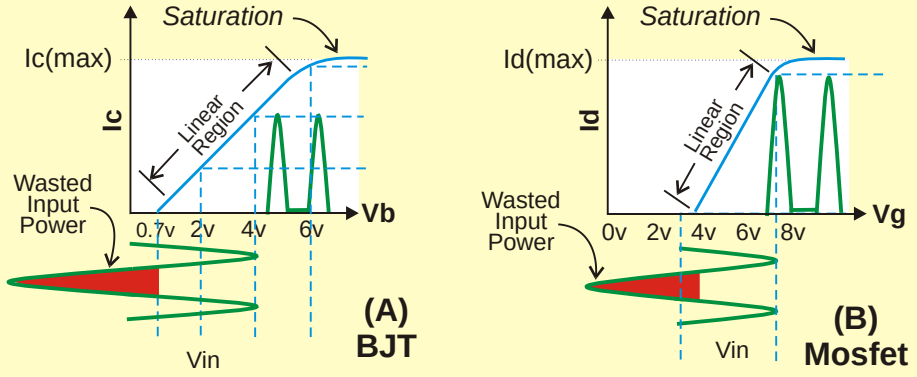


FIG. 1 – Class C Transfer Curves for (A) NPN bipolar transistor (self-biased) and (B) IRF510 mosfet at 3v gate bias

called the *gate threshold voltage*, or Vgs(th). From the IRF510 data sheet, the Vgs(th) is specified at 3.0v minimum to over 4.0v maximum. This large range is typical of mosfets, whose parameters tend to be quite sloppy compared to BJT's – something to always keep in mind. My experience shows the Vgs(th) of the IRF510 is more in the 3.7-4.0v range and goes into full saturation with about 8v on the gate. This defines a smaller dynamic range (4v–8v) for the linear region than a BJT (0.7v–8v).

The transfer characteristics of a typical IRF510 is shown in **Fig. 1B**. The gate is externally biased at 3v (no-signal) and the input signal is limited to no more than 7v on the peaks to avoid the saturation region. Note that the scaling between the BJT and mosfet transfer curves are different.

Class C PA with a BJT

Figure 2 is a schematic of a typical low power QRP transmitter PA using an NPN power transistor. RF input from the driver stage is stepped-down through T1 to match the very low input impedance of Q1, typically 10W or less. The low output impedance (12–14W at 5W) is converted to about 50W by the 1:4 step-up transformer T2. This circuit is the common *self-biasing* circuit -- there is no external dc biasing applied to the base, such that the signal voltage alone forward biases the transistor. Referring back to **Fig. 1A**, the shaded area of the input signal shows the power that is wasted in a typical Class C PA using self-biasing. This is power from the driver that *is not being used to produce output power*. This is an inherent short coming of the Class B and C amplifiers.

Class C PA with a MOSFET (IRF510)

The circuit of a typical mosfet **Class C** PA is shown in **Figure 3**. It appears very similar to the BJT circuit in **Fig. 2** in most regards. The RF input signal from the driver stage can be capacitively coupled, as shown, or transformer coupled. Capacitive coupling is easier for applying the external biasing. Since the Vgs(th) of an IRF510 is about 3.5–4.0v, setting of the gate bias, via RV1, should initially be set to about 3v to ensure there is *no drain current with no input signal*. R1 is chosen to simply limit RV1 from accidently exceeding 8v on the gate, which would cause maximum drain current to flow and certain destruction after 10–15 seconds. The input RF applied to the gate (during transmit) should likewise never be allowed to exceed about 7–7.5v, just shy of the saturation region. As illustrated, the input signal is 8Vpp, or –4v to +4v after C1, and after the +3v biasing, from –1v to +7v. *This ensures the IRF510 is operating within it's safe operating area* for a Class C amplifier. Like the BJT Class C PA, the input signal from +4v to –1v is wasted power, not being converted to output power.

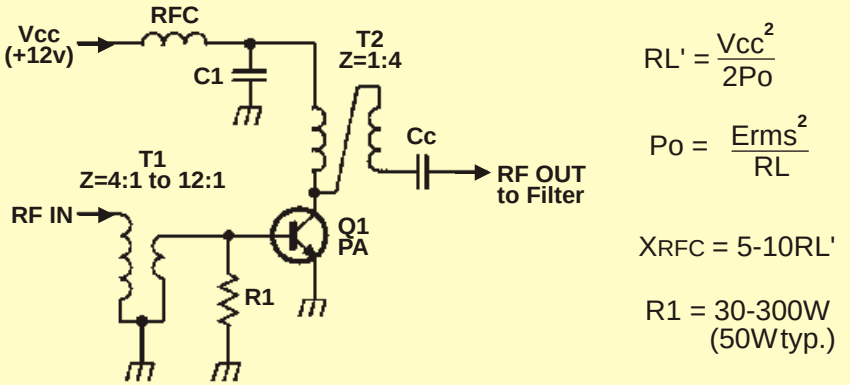
For a typical Class C PA operating at around 50% efficiency, about 850mA of drain current will be required to produce 5W output. It is wise to monitor the drain current to ensure excessive current is not being drawn, indicating the RF input peaks are not approaching the saturation region of the device, or the static gate voltage from RV1 is set too high. This is extremely important to preserve your IRF510 longer than a few moments!

Drain current will only flow when the gate voltage exceeds the Vgs(th) of the device. With a resistive drain load, this translates into +12v of drain voltage when no current is flowing, then dropping towards 0v as drain current flows, as shown in **Fig. 3**. However, with the inductive load of T1, the voltage swing will be 2Vcc (24v) as expected. This is due to the current stored in the inductance of T1 being dumped into the load (low pass filter) when drain current from the IRF510 stops, and is stepped up further, by a factor of two, to about 48Vpp, by the bifilar windings on T1. Some loss through the low pass filter yields about 45Vpp for 5W output.

Once the circuit is working properly, RV1 can be carefully adjusted to produce more power, again carefully monitoring for <1A of current flow. This is much easier to do with an oscilloscope, to ensure that the gate voltage never approaches the 7.5–8v saturation region on the RF peaks, and for a fairly clean sinewave entering the low pass filter.

Evaluating Class C MOSFET Efficiency

A well biased IRF510 PA can be a bit more efficient than a BJT circuit, primarily because it takes less peak-peak input signal to produce 5W, and thus less driver power is needed. Since the slope of the linear region is steeper than a BJT, the IRF510 actually has more potential gain.



$$RL' = \frac{Vcc^2}{2Po}$$

$$Po = \frac{Erms^2}{RL}$$

$$X_{RFC} = 5\text{-}10RL'$$

R1 = 30-300W
(50W typ.)

FIG. 2 - Typical BJT QRP Power Amplifier (PA) Stage

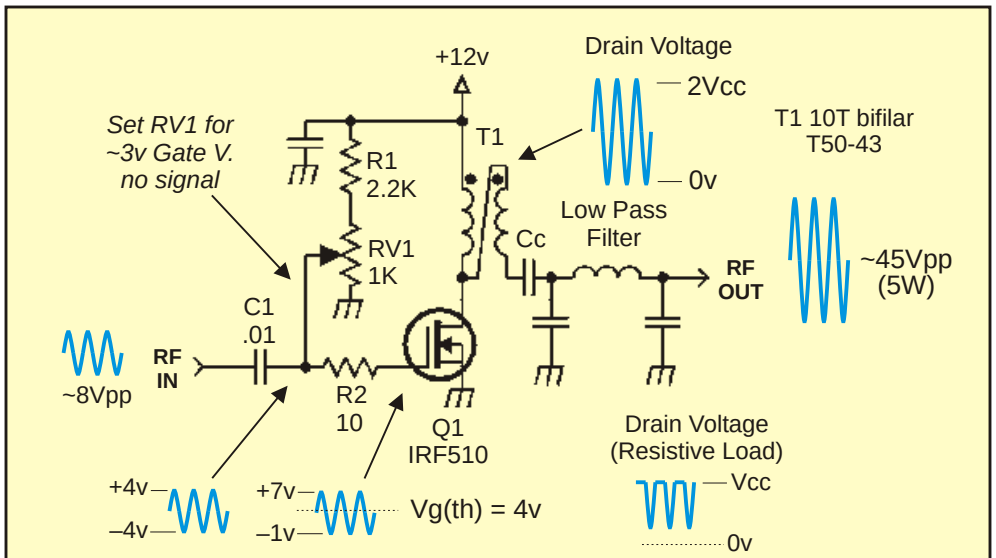


FIG 3 – Schematic of a typical MOSFET Class C PA

The largest contributors to power losses, and hence poor efficiency with switching mosfets, are the very large values of input and output capacitances compared to a BJT.

Remember how you've always heard the input impedance of a mosfet is very high, in the megohms? Well, forget you ever heard that! That is the *DC input resistance* of the gate with *no drain current flowing*. The AC input impedance is the Xc of Cin (about 120–180pF) or 130W at 40M (7 MHz). This means your driver stage must be able to provide an 8Vpp signal into a 130W load, or about *a half watt of drive*.

On the output side, the large output capacitance, *Cout*, is like having a 120pF capacitor from the drain to ground. This absorbs a fair amount of power being generated by the mosfet. But there is nothing you can do about that (at least in Class C).

The other large contributor to reducing efficiency is the power lost across the drain-source junction. This is true as well across the collector-emitter junction in a BJT. Power is E times I. The power being dissipated across the drain-source junction is the drain voltage (Vd) times the drain current (Id). When no drain current is flowing, there is no power being dissipated across the device, since +12v Vd times zero is zero. But for the rest of the sinewave, you have instantaneous products of Vd times Id. Looking at the mosfet again as a switch, this is known as the *transition loss,* as drain current is transitioning from it's OFF state (Id=0), through the linear region, to the ON state (Vd=0). Of course with Class C, you are in the transition loss region at all times while drain current is flowing. Again, there is little you can do about this loss in Class C amplifiers.

Improving Efficiency (Introduction to Class D/E/F)

From the above, it appears there are three major sources of power loss, leading to poor amplifier efficiency:

1) Transition (switching) losses (Vd x Id products)

2) Large internal gate input capacitance (~120-180pF for the IRF510)

3) Large internal drain-source capacitance (~ 120pF for the IRF510)

If these losses could be largely overcome, then the amplifier's efficiency could be greatly improved.

In class D/E/F, the mosfet is intentionally driven into saturation using a square wave. This drives the mosfet from OFF (Id=0), to fully ON (Vd=0) as quick as possible. The square wave input will have to go to ≥+8v to ensure saturation.

This purposely avoids the linear region, operating the device only as a switch. For this reason, Class D, E and F amplifiers are often called *switched mode amplifiers*, not linear amplifiers, as in Class A, B or C.

The transfer curves of a Class C vs. Class D/E/F PA with a square wave drive is shown in **Fig. 4**. The gate is biased at 3v in both cases, and Vgs(th) is 4v. The amount of wasted input power is greatly reduced with the square wave drive. The output will have a slope on the rising and falling edges, due to the short time drain current must travel through the linear region. Still, the ON–OFF switching action of these modes is evident.

A square wave is an infinite combination of odd harmonics. The square wave output must be converted back into a sine wave by removing the harmonic energy before being sent to the antenna

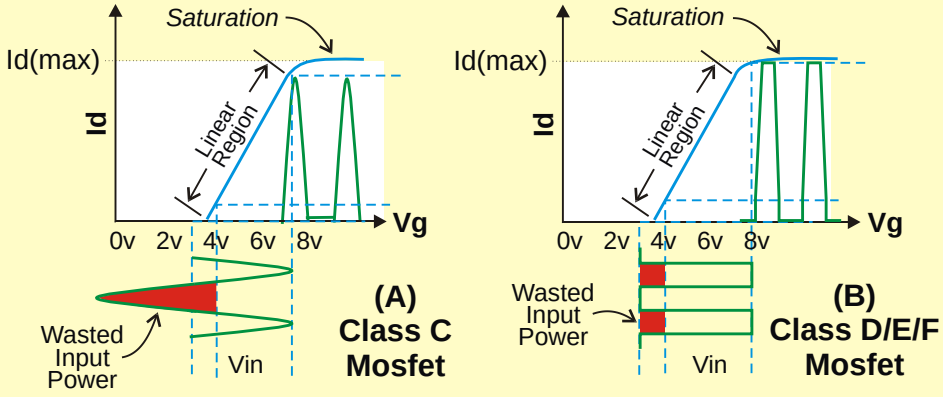


FIG. 4 – IRF510 Transfer Curves for (A) Class C Sine Wave Drive and (B) Class D/E/F Square Wave Drive

for FCC compliance. ***The method by which the fundamental frequency is recovered from the square wave output determines whether it is Class D, E or F.*** In all cases, it is based on driving the mosfet with a square wave input.

Legally, you can drive a mosfet into saturation with a huge sine wave as well, as many Class D/E circuits on the internet or ham radio publications are based. However, you are in the saturation region for a relatively short period of time (only during the positive input peaks), the rest of the time in the linear region. It is this authors opinion that the first step to increasing efficiency is avoiding the lossy linear region. This is defeated with a sine wave drive.

Therefore, the remaining discussion on Class D, E and F amplifiers are based strictly on a square wave drive.

It is worth mentioning an important distinction between the classes of amplifier operation. With *linear amplifiers*, the class of operation is based on the amount of time that collector or drain current flows: 100% for Class A, >50% for Class B, and <50% for Class C. However, the amount of time drain current flows in a *switched mode amplifier* has nothing to do with it's class of operation. It is based entirely on how the output power is transfered to the load and how harmonic power is removed.

CLASS D QRP PA

One implementation of a **Class D** QRP transmitter is shown in **Figure 5**. Note that there is little difference between the Class D PA, and the Class C mosfet PA shown in **Fig. 3**, other than being driven with a square wave and into saturation. One advantage of a square wave drive is it can be generated or buffered with TTL or CMOS logic components, making a 0v to 5v TTL signal, as shown. RV1 is again set for about 3v, which now corresponds to the 0v portion of the square wave, elevating the ON or HI portion of the square wave to +8v (+5V TTL + 3v bias), the minimum gate voltage to slam the mosfet into saturation. This is verified with an oscilloscope by monitoring the drain voltage, and noting that it falls nearly to 0v. A good IRF510 in saturation should drop to ≤0.4v.

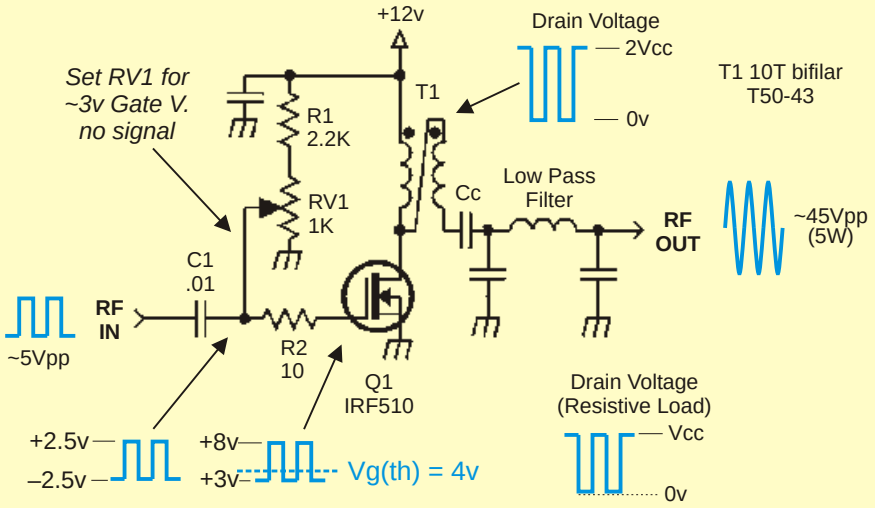


FIG 5 – Schematic of a typical MOSFET Class D PA

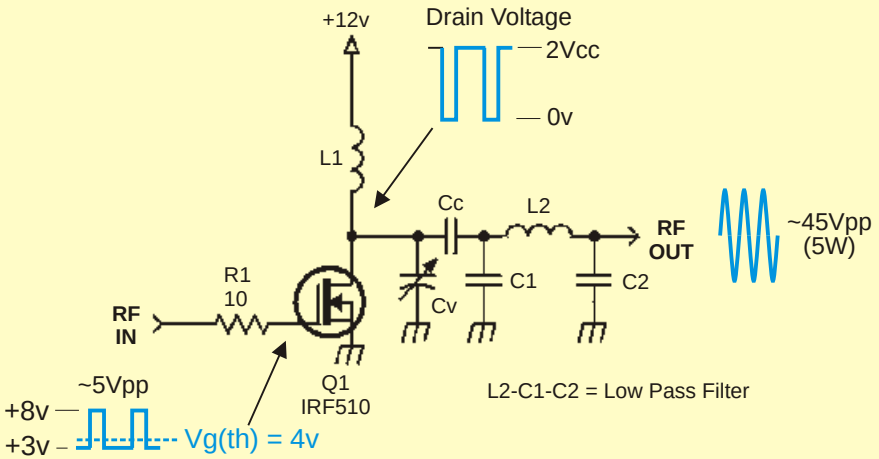


FIG 6 – Schematic of a typical MOSFET Class E PA

Speaking of oscilloscopes, having one is virtually required to properly build and tune Class D, E or F amplifiers. One must be able to see what the waveforms look like, the voltages, and the timing (or phase) relationships to ensure the amplifier is operating properly.

The output circuitry is also identical to the linear Class C amplifier of **Fig. 3**, impedance converted through T1, followed by a traditional reciprocal (50W in – 50W out) low pass filter. Input resistor R2 is a low value resistor, 3.9W to 10W, to dampen the input Q a bit and prevent VHF oscillations. The value is not critical. A ferrite bead could be used as well (but a small value resistor more available).

Controlling the Output Power of the PA

Note that the input signal, as shown in **Fig. 4**, depicts a square wave with a 50% duty cycle. One of the beauties of switched mode amplifiers is the ability to change the output power by changing the duty cycle of the input square wave.

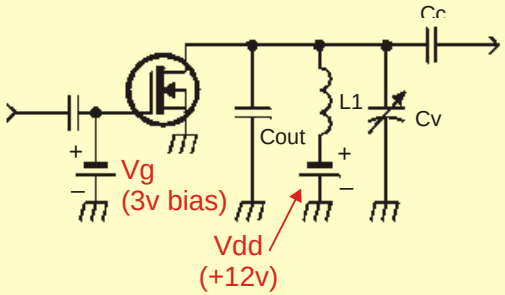
Remember that with an IRF510 in saturation, you are drawing the maximum rated drain current, about 4A. This, of course, is way too much current to draw for any length of time. With the circuit shown, 5W is produced with about a 30% duty cycle, drawing about 800mA of total transmit current (including driver stages) for an overall efficiency of ~70%. You are "pulsing" the 4A ON and OFF to produce an *average* desired current, and hence output power. The shorter period of time the mosfet is ON, the lower the average power.

Final thoughts on Class D

Class D amplifiers were initially developed for hi-fideltity audio amplifiers, converting the audio into pulse width modulation (PWM). Class D really defines an amplifier that uses PWM for generating *varying* output power, such as audio.

The basic fundamentals have been applied to CW RF amplifiers, by simply driving the mosfet PA into saturation. Since these amplifiers do not use a PWM input (since a CW transmitter demands a constant output power), they are not legally Class D. However, it has become accepted to refer to a mosfet PA, being driven into saturation *with standard low pass output filters*, as Class D.

For those wishing to experiment with these hi-efficiency switching amplifiers, start out with a simple Class D to see how they work and note the increase in efficiency. However, I would certainly recommend to any serious builder to graduate to a Class E PA.



Cout = Cds drain-source capacitance

FIG. 7 – Class E PA Parallel Equivalent Circuit

CLASS E QRP PA

The first **Class E** QRP transmitter to be considered is shown in **Figure 6**. The input is a 5Vpp square wave at the RF frequency, ranging between +3v and +8v due to the R1-RV1 bias network in **Fig. 5**, or as developed in the driver stage. The real difference, *which defines this circuit as Class E*, is the output side of the mosfet. A single inductor, L1, replaces the common bifilar transformer, and a variable capacitor, Cv, is placed from drain to ground. The output is capacitively coupled through Cc to the low pass filter.

To better understand this circuit, refer to the equivalent schematic in **Figure 7**. The IRF510 output capacitance, *Cout* or *Coss*, is 100-120pF, which would normally be an unwanted low impedance load to the drain circuit. However, in Class E, this output capacitance is used to our advantage by using it as part of a tuned circuit. Representing the +12v drain voltage as a battery, it can be redrawn to show how L1 is in parallel with *Cout*, forming a tuned circuit. Therefore, in Class E, the value of L1 is calculated to resonate with *Cout* at the desired output RF frequency. A fixed or variable capacitor, Cv, is usually added to the L-C circuit to

reach resonance at the transmit frequency. A parallel tuned circuit has very little net loss. Converting the mosfet's *Cout* from a loss element, to a low loss tuned circuit, is what *greatly increases the efficiency of this amplifier*. The current needed to charge Cout in Class E comes from the "flyback" energy of the tuned circuit, *not from the mosfet drain current.* In a properly tuned circuit, current flows through *Cout* only when the mosfet is OFF (no drain current flowing).

Table 1 – Initial Values

BAND	Cs	L1	WIND L1
80M	270p	5.0uH	10T T50-43
40M	120p	2.1uH	6T T50-43
40M	120p	2.1uH	20T T50-2
30M	120p	1.0uH	14T T50-6
20M	47p	0.8uH	13T T50-6
15M	—	0.5uH	10T T50-6

The combination of reducing the switching losses by using a square wave input, and reducing the effects of the internal capacitances, is what defines Class E.

Table 1 shows some initial starting values for the HF ham bands. *Cs* is the *total shunt capacitance* to add between the drain and ground – a fixed capacitor in parallel with the variable capacitor, Cv. On 40M, for example, this is a *total* drain-source capacitance of 240pF, including the internal *Cout* of the IRF510. The inductance, and the toroidal inductor to wind, is also shown to form the equivalent tuned circuit. I have built Class E PA's with these approximate values for all bands shown, except 80M, and all yielded an overall efficiency (total keydown current, including receiver and transmit driver currents) of at least 80%. However, these values need to be used with caution, primarily because the IRF510 *Cout* of 120pF, as listed on the data sheet, is for a Vd of +12v, that is, when the IRF510 is OFF. It rises to about 200pF as you approach saturation. The trick is to guestimate what the average IRF510 capacitance will be, depending on the duty cycle of the input square wave. To be truthful, it takes a little piddling around to get it right, but getting another percent or two of efficiency out of the PA is fun. In fact, it can become an obsession! Again, this is where an oscilloscope, and a power meter, is a must to tune the Class E PA for maximum efficiency. In practice, the *Cs* capacitance values listed in Table 1 will likely end up being a bit less than shown.

Note the square wave input shown in **Fig. 6** is depicted having a 30% duty cycle, not 50% in the Class D circuit. Output power is determined by varying the duty cycle of the input drive. With Class E, it is my experience that maximum efficiency occurs around 45% duty cycle of the input gate drive (45% ON, 55% OFF).

CLASS E QRP PA with Series Tuned output

Figure 8 shows another implementation of a Class E amplifier. Instead of using an LPF output filter, a combination of parallel and series tuned resonant circuits are used. As in the first example of the Class E amplifier, L1 forms a parallel tuned circuit with the total shunt capacitance of Cv and the internal drain-source capacitance of *Cout*. Instead of following this with a low pass filter, it is followed by a series tuned resonant circuit, consisting of L2 and C2. The combination of the two tuned circuits is sufficient to ensure FCC compliance for harmonic attenuation.

From my experience, the difficulty with this approach is selecting the component values to effect a proper impedance match to the 50W load. It can be done with a little math, computer modeling, or experimentation, but again, due to the uncertainty of the actual IRF510 *Cout* value and resulting average output impedance, a fair amount of tweaking is required. Once the output impedance is properly transformed into 50W at the antenna, and L2–C2 tuned for resonance, the efficiency will be about 85%. However, with the L2–C2 series tuned element, it becomes rather narrow banded and efficiency drops when the frequency is moved about 10KHz. A variable capacitor across C2 will allow retuning upon frequency changes, although in practice, this is cumbersome for the way most of us prefer a no-tune QRP transmitter.

There are still other ways to implement the Class E amplifier, such as additional parallel or series tuned circuits on the output, or using impedance transformation schemes. It is an area worthy of further development by hams and QRPers. The main goal is to use the internal drain-source capacitance as part of the parallel tuned output circuit with the drain inductance. This will generally require some additional capacitance between drain and ground, and some means to tune it to resonance. By doing so, the output capacitances are charged from the "flywheel effect" of the tuned circuit, that is, current from the drain inductor, not from the drain current. The later is wasted energy, which lowers the efficiency.

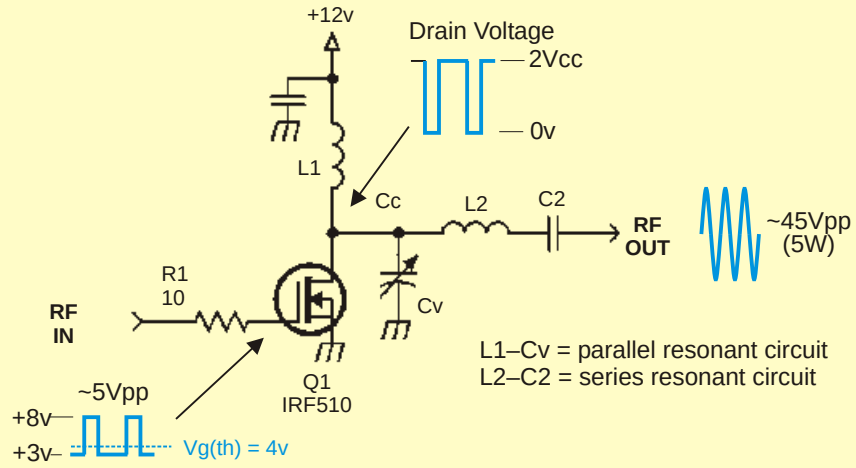


FIG. 8 – Class E Transmitter with Series Tuned Output

CLASS F QRP PA

The square wave *drain voltage* is rich in odd harmonics, predominantly the 3rd and 5th harmonics (3fo and 5fo). A sinewave with odd harmonics will be flattened at the peaks (at 90º and 270º), lowering the efficiency of the PA. Upon removing the odd harmonics, it will be a proper sinewave. In a typical QRP transmitter, the harmonic power is thrown away by the low pass filter. However, if one were to use this odd harmonic power in proper phase, the power could be added to the fundamental frequency to boost the output power. This would increase the efficiency of the amplifier.

This is the essence of Class F. The output network consists of odd harmonic peaking circuits in addition to

resonant circuits at the desired fundamental frequency. This forms the clean output sine wave, and the odd harmonic peaking adds a bit of power to the fundamental to increase PA efficiency.

Figure 9 shows one approach to accomplishing this. Component values are chosen such that L2–C2 is resonant at the 3rd harmonic, and L1–C1 and L3–C3 resonant at the fundamental frequency.

To analyze the circuit, consider the functions of these networks at different frequencies.

At the 3rd harmonic (3fo), L2–C2 is resonant, their reactances cancel out, offering little resistance to the 3fo voltage, passing the 3fo power to the L3–C3 network. L3–C3 will appear capacitive at 3fo, and will be charged with the 3fo power.

At the fundamental frequency (fo) L3–C3 is resonant, with a slight boost in power due to the voltage added to the network by the 3fo peaking circuit described above. At fo, L2–C2 (fr=3fo) will appear inductive, and the value of C1 is selected to form a series resonate circuit at the transmit frequency with this inductance. Normally, C1 is a dc blocking capacitor, usually 0.1lF. In Class F, C1 will be a few hundred pF, depending upon the fo.

Obviously, it takes some math to figure out these values for the respective resonances, and to achieve the proper impedance transformation to a 50W load.

I have built several Class F amplifiers, using an impedance network analyzer to verify the impedances, capacitance and inductance of all elements at fo, 2fo and 3fo. Inspite of being properly tuned, I have never been able to reach an efficiency higher than what I've obtained with Class E. It is my opinion that the extreme complexity of Class F is not worth the effort over Class E *at QRP levels*. Class F is used in commercial 50kW AM transmitters, and at even higher powers for shortwave transmitters. Perhaps the extra 1–2% of efficiency is worth it for saving a kilowatt at these power levels, but is scarcely measurable at QRP powers.

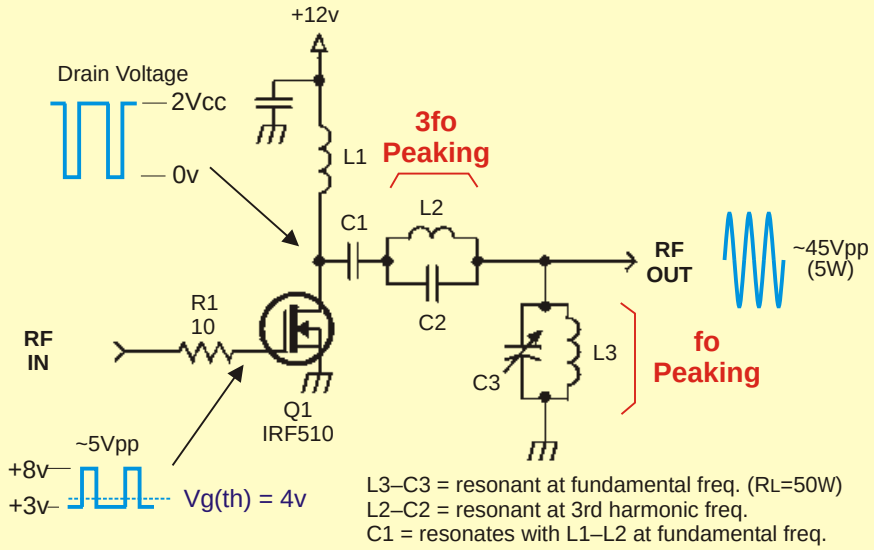


FIG. 9 – Class F Transmitter with Harmonic Peaking

None-the-less, Class F is a clever approach to increasing efficiency, and presented here for sake of completeness of the high efficiency modes.

Conclusion.

These switched mode PAs are ideal for QRP and the homebrew construction of low power transmitters, in that the higher efficiency directly relates to lower battery drain. It is worthy of further development by QRPers and experimenters, and the reason the theory has been presented in the first part of this article.

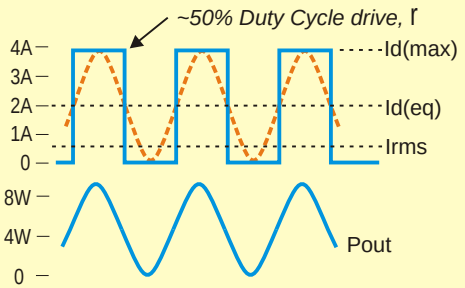
In **Part 2** – a more technical approach to Class D/E/F will be presented, along with details of the gate input drive requirements and suitable driver stages, with actual oscilloscope waveforms. The IRF510 Data Sheet is also included in Part 2. sometimes more!)

For those interested in Class D/E/F, I hope you have found the information in Part 1 of this tutorial informative. For those of you building such circuits, I would be interested in hearing of your success and approach.

72, Paul Harden, NA5N
na5n@zianet.com
pharden@nrao.edu

Appendix A – Pulse Width Modulation (PWM) or varying the duty cycle to control output power

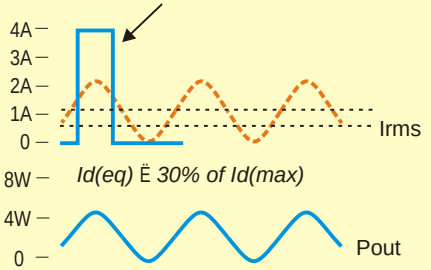
50% Duty Cycle Drive



Consider the drain output current above with a 50% duty cycle and the IRF510 Id(max) of 4A. The sinewave equivalent is shown as the dotted wave-form. Id(eq) is effectively converting the peak-to-peak current to peak current (at 50% duty cycle), then converting to Irms to determine output power, as calculated below.
r = duty cycle, g = PA efficiency

Id(eq) = r Id(max) = 50% x 4A = 2A
Id(avg) = .637Id(eq) = .637 x 2A = 1.3A
Irms = .707Id(avg) = .707 x 1.3A = 0.9A
Po = IrmsVddg = 0.9A x 12v x 80% = 8.8W

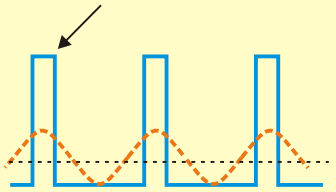
30% Duty Cycle Drive



Id(eq) = rId(max) = 30% x 4A = 1.2A
Id(avg) = .637Id(eq) = .637 x 1.2A = 0.76A
Irms = .707Id(avg) = .707 x 0.76A = 0.54A
Po = IrmsVddg = 0.54A x 12v x 80% = 5.2W

20% Duty Cycle Drive

What is the Output Power at r= 20%?



The Handiman's Guide to

MOSFET "Switched Mode" Amplifiers

Part 2

Gate Input & Drive Requirements

(Or, Mosfets for the Obsessive Compulsive)

by Paul Harden, NA5N

__Part 2__ is for those with a desire to design and build Class D/E/F amplifiers. The following information, of a more technical nature than Part 1, may be found to be useful for understanding the gate input requirements and some driver circuits.

MOSFET Capacitances

Figure 10 is a graphical representation of the capacitances in a switching MOSFET. An understanding of these capacitances is important for properly driving a class D/E/F PA. **Figure 11** shows the nominal values of these parameters for the IRF510.

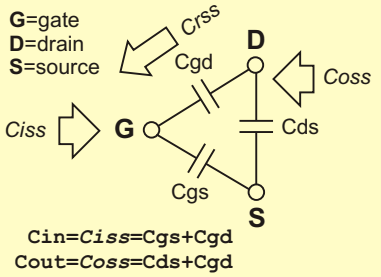


Fig. 10 – MOSFET Capacitances

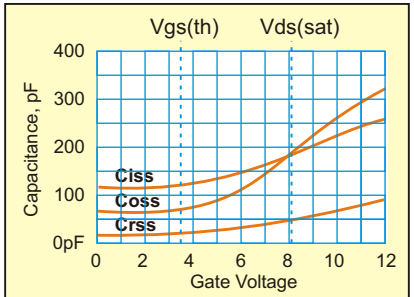


Fig. 11 – IRF510 Capacitances

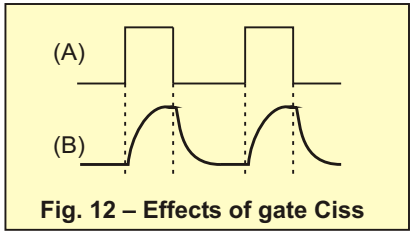


Fig. 12 – Effects of gate Ciss

Input Capacitance, *Ciss*, is the gate-source capacitance, *Cgs*, plus the reverse transfer capacitance, *Crss*. For the IRF510, *Ciss* is ~120pF when the device is OFF, increasing to ~180pFwhen the device is ON, due to the influence of *Crss* and the drop in drain voltage.

Applying a square wave to the gate, *Ciss* must charge before the voltage appears across the gate-source junction. This is illustrated in **Figure 12**, where (A) is the input square wave, and (B) is the true gate voltage, that is, the voltage impressed across the internal gate capacitance. The resulting drain current would appear virtually the same as waveform (B).

Once *Ciss* charges to Vgs(th), about 4v for the IRF510, drain current begins to flow and a portion of the output capacitance, *Coss*, is reflected back to the gate in the form of the reverse capacitance parameter, *Crss*. This

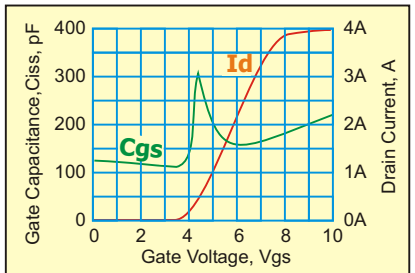


Fig. 13 – Gate voltage vs. Ciss and Drain Current (Id)

(and other factors) causes a sudden increase in the gate capacitance at Vgs(th). This is illustrated in **Figure 13**, with Vgs(th) at 4.0v. The graph is derived from the data sheets, application notes, and measurements I have made on the IRF510.

This rather complex input capacitance graph is not shown in **Fig. 11**, as most data sheets show only the *average* capacitance over the gate or drain voltage range, not the aberration that occurs when drain current first begins to flow. This is important to realize, as it alters the actual gate voltage waveform one will observe on an oscilloscope when driving with a square wave.

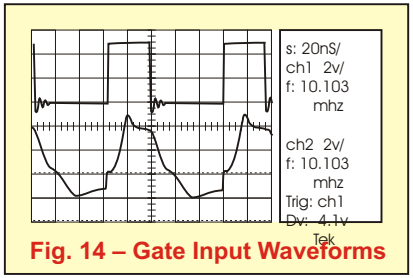


Fig. 14 – Gate Input Waveforms

Figure 14 is an oscilloscope display showing the waveforms one can expect. The gate waveform serves as a great diagnostic tool in evaluating your class D/E/F transmitter.

I drive the mosfet with a low-Z emitter follower. The top trace (Ch.1) shows the input to the emitter follower, a fairly pure square wave at 10.103 MHz on a 30M transmitter. The bottom trace (Ch.2) is the gate waveform. The gate is biased at 3vdc, such that the TTL square wave drives the gate from about 3v, below Vgs(th), to a little more than 8v for saturation. When the square wave goes from LO to HI, the gate voltage immediate rises to 4.2v, where it hesitates – a visual indication of the actual gate threshold voltage, Vgs(th) for this device. This is the point where drain current begins to flow. The slower slope between Vgs(th) and 8v is due to the increased *Ciss* above Vgs(th) on **Fig. 11**. This is also the area of maximum gain of the device. The desired flattening out of the gate drive at 8v indicates the mosfet is in saturation, although this is confirmed by monitoring the drain voltage, as discussed later.

When the gate drive goes from HI to LO, gate voltage returns to the 3v bias level rather sluggishly, due to *Ciss* discharging. Note that at Vgs(th), the falling waveform again changes it's slope – due to *Ciss* being altered by the gate junction storage charge effect when gate voltage falls below Vgs(th).

Gate Driver Considerations

Of importance in class D/E/F is the time to reach Vgs(th), the gate threshold voltage, after application of the gate drive going HI. This is described by:

$$t = \frac{Ciss \times Vgs(th)}{Ig}$$

Solving for gate current, Ig:

$$Ig = \frac{Ciss \times Vgs(th)}{t}$$

The above equation indicates that the higher the gate current, provided by the driver stage, the faster *Ciss* will charge, and the higher the efficiency of the PA.

For class D/E/F, the point of the square wave drive is to get through the linear region as soon as possible. This

means *Ciss* should be charged as quickly as possible.

I recommend striving for 15–20nS. See **Figure 15**. This is also consistent with the ~16nS rise time, tr, of the IRF510. "Tr" is theoretically the fastest *Ciss* can be charged.

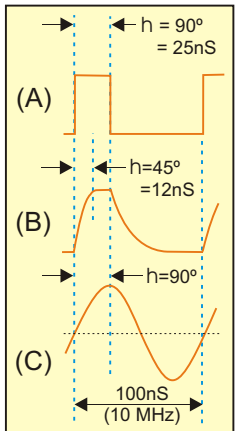


Fig. 15
Driver Timing

The figure shows the input gate drive (A) being a 25% duty cycle, or 90º of the RF cycle. At 10.1 MHz, the gate drive "pulse" would be about 25nS, and to charge *Ciss* two times faster would indicate 12nS, as shown in (B). From the previous equation, this would indicate a gate current of 50mA is required. This is a bit high for QRP!

I have found a driving current of 25-30mA to be a nice compromise to charge *Ciss* sufficiently fast for high efficiency. Referring to **Fig. 15 (B)**, if the gate waveform does not flatten out at the 8v level (looks more like a sine wave), the driver is not providing sufficient current to the gate. Driving the gate voltage to saturation quickly, by providing sufficient gate drive current, *is paramount in achieving the high efficiency of class D/E/F.* The 25mA of drive current will save 200mA or more of PA current at 5W QRP. Observing the o-scope drive waveform in **Fig. 14**, note that *Ciss* charges in 18-20nS at 10.1 MHz This 30M transmitter has an overall efficiency of 82%, which *includes* the 40mA of key-down current due to the TX mixer, comparator and emitter follower driver providing the gate current. This same 18-20nS Ciss charge time will cause a lower efficiency on 20M, as it's approaching the period of the RF. At 40/80M, this 18-20nS rise time will produce higher efficiencies, since it is a smaller percentage of the RF cycle at lower frequencies..

Also note that the input gate square wave in **Fig. 14** is about a 30% duty cycle – 30% ON and 70% OFF. The output power from the class D/E/F PA is determined by the duty cycle. With the IRF510, a 15% duty cycle produces about 1W output; about 5W at 30%, and 8W at 45%. Efficiency begins to drop above 45% duty cycle .

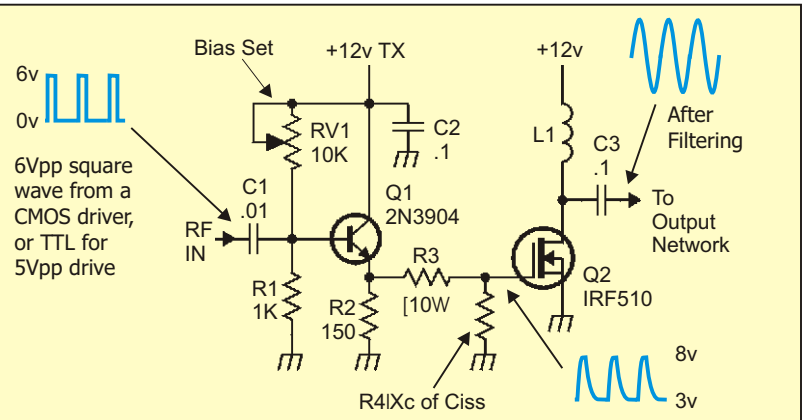


Fig. 16 – Low-Z Emitter Follower MOSFET Driver

25mA Emitter Follower Driver

The square wave drive can be developed by some type of CMOS or TTL gate. These alone do not have the current sinking capabilities needed to properly drive the IRF510. Some type of current booster, plus the ability to shift the dc level of the input square wave is required. The emitter follower circuit in **Figure 16** is one approach. This works best if you provide a 6V square wave to Q1, such as from a 6–8v CMOS gate, rather than 5V TTL. This is due to the 0.7v drop in the emitter follower, leaving only about 4V from a TTL drive. This may not drive the IRF510 into saturation.

The input square wave is dc shifted by C1 (dc blocking) and the RV1–R1 bias network. Adjust RV1, by monitoring the gate on an oscilloscope, as follows: when the input square wave is LO, the voltage on Q2 gate should be about 3v; when the input goes to +6v HI, the gate voltage should be between 8–9v, depending upon the loading to the circuit. This 3–8v output is developed across R2 and R4. The 3v level is to ensure the IRF510 is OFF, <Vgs(th), and 8v for saturated ON.

Q1 is powered from the +12v TX term to shut down the driver in receive, in the event RV1 is misadjusted to cause mosfet drain current to flow when the mosfet should be OFF.

R3 is 3.9–10W to de-Q the gate and prevent VHF oscillations. The value is not critical. R4 is a resistive load to both the Q1 emitter follower and Q2 gate. The value should be about the Xc of the mosfet *Ciss*, ~120–180pF, or a few hundred ohms, depending upon the transmit frequency. Initially, you can make R4 a trim pot and adjust for the best possible square wave (**Fig. 14**) to match to the *Ciss* of the IRF510. This value will vary from device-to-device.

If the rise time is slower than 25-30nS, then more gate current is needed by decreasing the value of R2. In this example, if a 3v-to-8v signal is formed across R2, then the output drive current would be about 33mA on the drive peaks. (I=5V/150W). Ohms law is thus used to determine R2 for the drive current desired.

In the technical literature, the following equation is used to calculate the driver resistance, Rd, needed (R2 in **Fig. 16**):

$$Rd = \frac{-t}{CissLn(1-V2/V1)}$$

Where, t is the desired rise time of the gate signal (usually 15-20nS), V1 is Vg at saturation, V2 is the peak-to-peak gate voltage, or V1 minus Vgs(on), and Ln is the *natural* logarithm. For the driver in **Fig. 16**:

$$Rd = \frac{-t}{Ciss\ Ln(1-5v/4v)}$$

$$= \frac{-20nS}{120pF(-1.38)} = 120W$$

Keep in mind, this value of Rd is based on the ideal current to charge *Ciss*, about 50mA. Again, I have found 25-30mA to be sufficient. This exercise does show that using Ohms Law for R2 is close enough (and a lot easier!).

The NA5N Mosfet Driver

Another driver scheme developed for my class D/E transmitters is shown in **Figure 17**. It is similar in some regards to the emitter follower driver in **Fig. 16**.

The low-level RF output from the TX mixer is applied to a high speed comparator, which converts the RF sinewave into a square wave. The operation of the TX mixer and comparator is beyond the scope of this part of the article, but will be presented in a class D & E transmitter construction project in Part 3. Suffice it to say that the duty cycle of the square wave is variable from about 15–45%. The

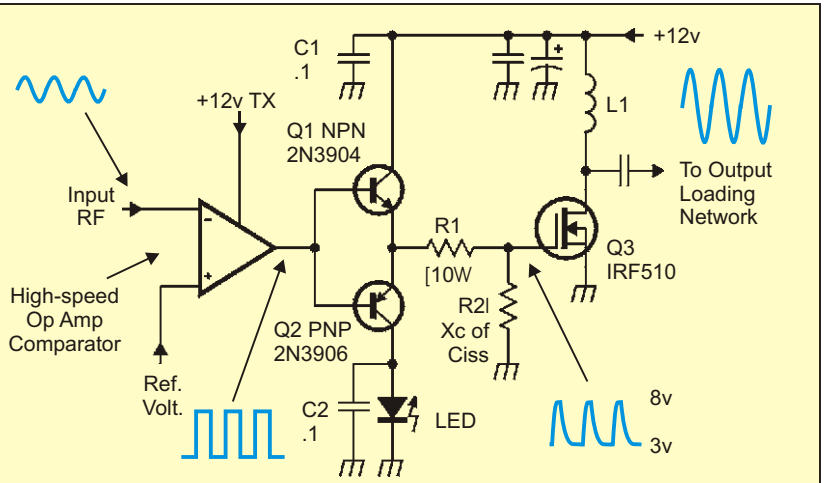


Fig. 17 – NA5N NPN-PNP Emitter Follower Mosfet Driver

comparator is powered from +12v TX, so that during receive, the output is 0v, disabling the IRF510 drive circuitry.

On transmit, the comparator output is an 8Vpp square wave at the RF frequency, such that the dc output levels are about +1v LO to +9v HI.

This emitter follower is an NPN-PNP pair, commonly called a "totem pole" configuration. Since the base voltage is an 8v square wave, the transistors are driven nearly into saturation and cutoff, acting as switches. When the comparator output goes from LO to +9v HI, both the NPN and PNP are turned on. Q1 emitter voltage is the +9v base voltage, minus the 0.7v junction drop. This 8.3 volts is applied to the emitter of Q2, allowing it to be forward biased as well. The 8.3v is also the PA gate drive. R1+R2||Xc is the output load to Q1 and the input impedance to the IRF510, such that the impedance is self matching. This yields 25–30mA of gate current drive from Q1. About 8mA passes through Q2, illuminating the LED.

When the square wave goes to +1v LO, Q1 and Q2 are barely forward biased and conducts ~8mA due to the LED. This causes a 2v drop across the LED, and ~1v across Q2, leaving +3v at the Q1-Q2 emitters – and the mosfet gate – turning off the IRF510.

Even though there is only 2.5v drive to the IRF510 gate, the +8v previously on the gate *Ciss* is now discharging. This decaying gate voltage also appears on the Q1-Q2 emitters. The low Q2 emitter-collector resistance, which is in parallel to R2, gives *Ciss* a lower resistance to discharge into. When *Ciss* is discharged, Q2 turns off. Thus, the purpose of Q2 is to place a low-Z load across the IRF510 gate to quickly discharge *Ciss* when the mosfet turns off.

For class D/E/F efficiency, the drain

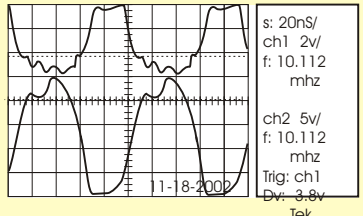


Fig. 18 – Gate/Drain Waveform

current must be zero before the next square wave LO to HI transition occurs.

Figure 18 is an oscilloscope display of this circuit driving a class E transmitter. The top trace is the **gate voltage** at 2v/div. Vgs(th) of this particular device is 3.8v, shown by the dotted line marker on the oscilloscope. Gate voltage rises fairly quickly to saturate at 8v. When the drive signal switches from HI to LO, the action of Q2 discharges *Ciss* and drops the gate voltage below Vgs(th) faster than the emitter follower version in **Fig. 16**. In this case, R1=3.9W and R2=220W.

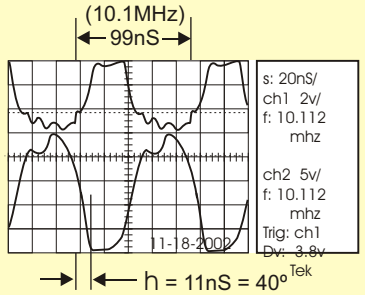
Gate voltage settles out around 2.5v, due to the LED and Q2, keeping the IRF510 turned off. If the gate were allowed to discharge to 0v, it would take longer to charge *Ciss* when the next gate drive goes HI. This saves 2.5v of *Ciss* charging. The main purpose of the LED is to provide this gate bias when the mosfet is off. Of course it does make for a nice XMIT indicator as well, indicating RF is being supplied to the IRF510, rather than simply coming off the key line.

The bottom trace is the **drain voltage** (Vd) at 5v/div. The peak-to-peak voltage is about 25v, the 2Vcc (or 2Vdd) expected. Note that when the gate voltage reaches +3.8v Vgs(th) going HI, the drain voltage is just passing through 12v Vcc – the point when drain current is zero. This is exactly the point you want the gate voltage to reach Vgs(th) to start drain current to flow. Vd drops from 12v down to 0v, indicating drain current is increasing. When the gate voltage reaches 8v, drain current should be saturated, evidenced by Vd reaching ~0v. In this case, Vd=0.4v, certainly indicating the IRF510 is in saturation, or the "full-ohmic on" region. This is important, as the closer to 0v at maximum drain current, the smaller the power losses across the drain–source junction. The lower the loss, the higher the efficiency. The drain current is also building up the current field in inductor L1 at this time. If drain voltage does not reach <1v, the mosfet is not in saturation.

When the gate voltage begins it's HI to LO transition, to turn OFF the mosfet,

Calculating PA Efficiency

PA efficiency of class D/E/F can be easily measured on an oscilloscope by measuring the LO to HI gate drive transition to the point the drain current first saturates (when drain voltage hits the lowest value). This accepted method is basically a measure of how long you spend in the linear region. The time to reach saturation is compared to the time of the RF cycle to determine the phase delay, in degrees. The steps to calculate PA efficiency, based on the NA5N driver and PA waveform in **Fig. 18**, are shown below. Calculating efficiency based on measuring PA currents (input vs. output power) yielded 91%.



❶ Measure time difference (in nS)

❷ Convert to phase difference (degrees)

$$h = \frac{11nS}{99nS} = .11x360^o = 40^o$$

❸ Calculate PA efficiency, g

$$g = \frac{\sin h \times 360^o}{2\pi h} \quad \text{where } \sin 40^o = .64$$

$$g = \frac{.64 \times 360^o}{6.28 \times 40^o} = \frac{230}{251} = 92\%$$

drain voltage begins to rise, indicating drain current is turning off as desired. Gate voltage drops from +8v to +3.8v Vgs(th) faster than the single emitter follower waveform in **Fig. 16**, due to the loading effect of Q2. Drain voltage rises above 12v Vdd as the current stored in L1 now dumps into the output network when drain current stops.

In class E, L1 is also part of the output tuned circuit, resonant at the transmit frequency by the shunt capacitor in conjunction with the internal *Coss*. See "Cv" in **Fig. 6, Part 1**. When the current stored in L1 is depleted, drain voltage will begin to decrease. However, in class E, the energy stored in the capacitor parallel to L1 will provide voltage when the current in L1 is depleted, causing the familiar "fly-wheel" effect of the resonant circuit. In **Fig. 18**, the hesitation in drain voltage at 20v is when L1 runs out of current, and the voltage peak to 25v is the voltage being supplied by the shunt capacitor, which has been charged to 2Vdd. Two or three peaks may be seen at the 25v level, depending upon the harmonic power present. With this waveform, the transmitter had a power range of 1W to 9W (by varying the duty cycle from 15% to 45%) with an overall efficiency of 85% and a PA efficiency of 92%.

Class D Drain Output Efficiency

The output capacitance, *Coss*, lowers efficiency, since it must be charged to ~2V_{DD} by the mosfet. The equations below show how efficiency, , is based on the switching power, Ps, lost across *Coss*. The following math only serves to make two important points below.

At V_{DD}=12v, for a 20M 5W transmitter, with Cs=120pF and Vsat=0.5v (where

$$Veff = V_{DD} - Vsat = 12v - 0.5v = 11.5v$$

$$Ps = Coss(2Veff)^2 \times 2fo =$$
$$= 120pF(2*11.5)^2 \times 2(14MHz) = 1.78W$$

$$= \frac{Po}{Po+Ps} = \frac{5W}{5W+1.78W} = 74\%$$

Ps is the switching loss in watts):

In some of the amateur literature, the recommendation is sometimes given to raise the mosfet drain voltage for higher efficiency. Let's see if this is true.

$$Veff = 18v - 0.5v = 17.5v$$

$$Ps = 120pF(2*17.5)^2 \times 2(14MHz) = 4.1W$$

$$= \frac{5W}{5W+4.1W} = 55\%$$

At V_{DD}=18v, to produce 5W output power:

Increasing V_{DD} to 18v does produce 5W with less drain current. However, charging *Coss* to 36v (2V_{DD}) greatly increases the switching power loss, lowering efficiency from 74 to 55%. This should dispell the rumor that increased V_{DD} lowers efficiency – and that the +12v customarily used by homebrewers is actually quite ideal for switching mosfet QRP PAs.

The second point with the above equations is how the *switching losses are frequency dependent*, due to the term "2fo." The lower the frequency, the lower the losses, and hence higher efficiency. Therefore, a Class D/E/F PA will be much more efficient on 80M than 20M. This is why most Class E circuits on the internet are only for 160M or 80M, as even a sloppy job of designing the circuit and using a sinewave drive

$$Veff = 12v - 0.5v = 11.5v$$

$$Ps = 120pF(2*11.5)^2 \times 2(1.8MHz) = .23W$$

$$= \frac{5W}{5W+.23W} = 96\% \text{ !!!}$$

will still yield high efficiency. Re-calculating the 20M 12v QRP example to 160M yields an astounding 96%. This is also why those scaling these amplifiers for 20M have had disappointing results, as the switching power losses double as you double the operating frequency.

A few loose ends ...

IRF510 vs. IRL520

The IRL520 is a logic family mosfet, meaning it is designed to saturate with only 5V (TTL logic HI) on the gate. It would therefore seem the IRL520 would be ideal for a class D/E/F PA for QRP, since it can be turned on with only a 2v swing on the gate. However, the input capacitance, Ciss, for the logic drive devices is very high – in the order of 300-400pF. This is tolerable for their intended purposes in 50-100 KHz switching power supplies, but virtually impossible to drive at HF frequencies. I have built some fairly successful Class C PAs with IRL520's, but efficiencies at Class D/E/F never much more than 50%. Theoretically, one can drive the gate with a parallel inductance to cancel out this huge capacitance through resonance, but I have not yet tried this. There are some SMC SOT-23 logic mosfets with a lower *Ciss* worth experimenting with.

Other switching MOSFETs

Just look through the Mouser or Digi-Key catalog and you will see listings for legions of cheap, switching mosfets. Many can be used in lieu of the IRF510. In order to use them for Class D/E/F, you need to know primarily the Vgs(th), Vg(sat), and output capacitance, *Coss* or *Cds*. Maximum drain current is also important. For QRP power levels, you want a device with a Id(max) of 1-2A for smooth power control with a 50% duty cycle, since you are forcing maximum Id for some period of time. The IRF510 Id(max) is about 4A. Such a high Id(max) actually makes the IRF510 a bit difficult to control in the 5W or less range.

Surface Mount MOSFET's

Some of the switching mosfets that meet the above requirements are only available in surface mount packages, such as SOT-23's with Id(max) around 1.5–2A. I have built a class D and E PA with these devices with good success, and surprisingly, the high efficiency causes little heating of these very small packages. However, operating them Class C causes excessive heating above about 2W. There is just very little room for error with a SOT-23 due to the low power dissipation of such small physical packages.

Other available literature

There is plenty of available information on Class D/E/F transmitters on various websites, engineering magazine articles and the application notes in National and Motorola data books. However, this information needs to be used with caution for QRP, as most are based on RF type switching mosfets, deal with power ranges in the hundreds of watts, push-pull circuits, or frequencies below HF, such as for AM broadcasting or ultrasonic use. Still, these articles are worth further study for those wishing to learn more, keeping the application of the article in mind.

Interpretting the IRF510 Data Sheet

The data sheet for the International-Rectifier IRF510 is in **Appendix B**. This is extracted from their complete data sheet.

Maximum Ratings. Continuous drain current is important, as this is about the drain current for the period of time the IRF510 is in saturation. This should stress why controlling output power with a small duty cycle is important. Maximum gate-to-source voltage is !20v, which will easily handle the +10v required for saturation.

Electrical Characteristics. **$R_{DS(on)}$** is the "on-resistance," which only occurs when fully saturated. Note the Test Conditions define the saturated

state with VGS=10v. When in the linear region, RDS is the standard equation for RL = Vdd^2/2Po.

Vgs(th) is the gate voltage where drain current begins to flow. Note the huge range - typical of mosfets. Most devices will be about 3.5-4v. **LD** is the internal inductance that adds to the external inductance on the drain. In class E, where the drain inductance forms a tuned circuit, the value of LD is sufficiently low to not alter calculations. **Ciss** and **Coss** are the input and output capacitances. These are very important, especially for class D/E/F. Note the test conditions are for Vgs=0v, that is, with no drain current flowing. With drain current, Vds will drop from +12v to 0v (at saturation) and these values change, as shown in **Fig. 3** on the data sheet. Timing parameters, **Td(on)**, **Tr** and **Td(off)** are defined in **Fig. 6**. For class D/E/F, the faster the better. Theoretically, the fastest a mosfet can switch is the time of Tr+Tf+Td(on)+Td(off), which equals 54nS for the IRF510. Tf is assumed to be about Tr if not listed. The maximum frequency would thus be 1/54nS = 18.5MHz. Tr and Tf define the typical time to charge and discharge Ciss and Coss. These times can be increased a bit by increasing the gate drive current, as discussed in the article, and raising fmax to some extent.

Fig. 1 shows drain current (Id) vs the drain-source voltage (Vds) at 25ºC. This is similar to the transfer characteristic curves for a BJT. **Fig. 2** is the same, except at a device temperature of 175ºC. Note that as the IRF510 gets hotter, drain current gets less, protecting itself from thermal runaway. This is opposite the effect of a BJT, where the BJT gets hotter, more collector current flows, producing more heat, then more current, until the device destroys itself by thermal runaway. Again, a mosfet protects itself from thermal runaway. This explains why your class C IRF510 PA drops in output power as the device gets hot.

Fig. 4 is the transfer characteristics of the IRF510. This shows how much drain current flows vs. the gate voltage. Note that the graph begins at 4v, as less than that, the mosfet is in "cut off." Also note the drain current is less at 175ºC. This shows how device saturation occurs around Vgs=8v, where little further increase in drain current occurs with increasing Vgs. Below Vgs=8v is the linear region, although it is not very linear (more "curved" in shape). The transfer curve is steepest between about 4 to 5v Vgs. This is the area of maximum gain. This shows why IRF510s have also been used as very high gain RF amplifiers or mixers, by exploiting a gate voltage only slightly above Vgs(th).

Fig. 5 shows the maximum drain current vs. temperature. For class C QRP transmitters, device temperature can quickly rise to 150ºC on key down, but still in the safe operating region for 1A of drain current. Class D/E/F runs considerably cooler. In fact, a barely warm IRF510 after 30 seconds of keydown is the ultimate proof of the increased efficiency. Try that with class C and you'll loose your fingerprint!

In **Part 3** of this series will be two construction projects for you to build – a QRP Class D and E transmitter using the IRF510. Both can be added to about any QRPp transmitter to produce 5W output, or for a "roll-your-own" transmitter.

72, Paul Harden, NA5N
na5n@zianet.com
pharden@nrao.edu